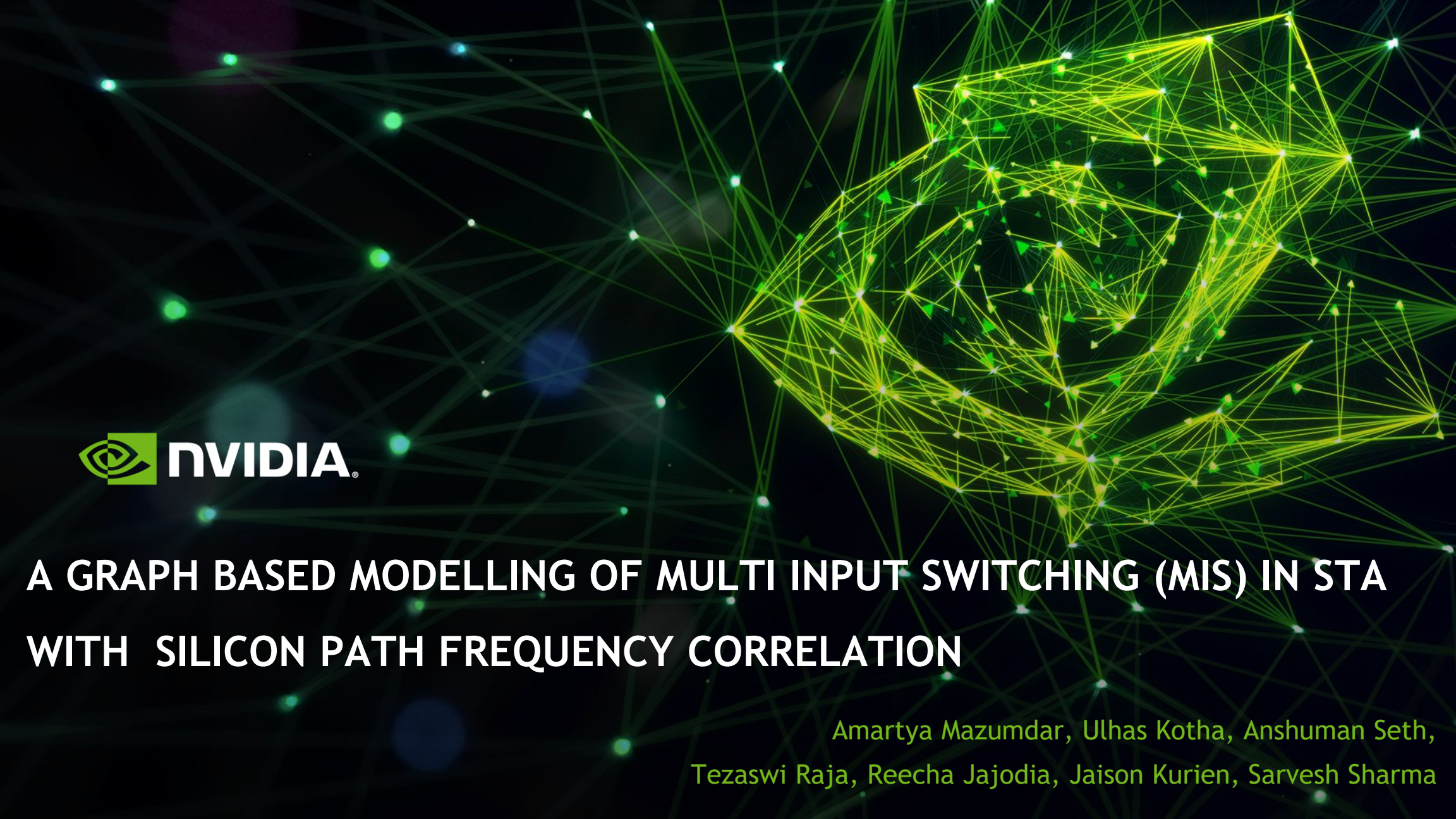

A GRAPH BASED MODELLING OF MULTI INPUT SWITCHING (MIS) IN STA WITH SILICON PATH FREQUENCY CORRELATION

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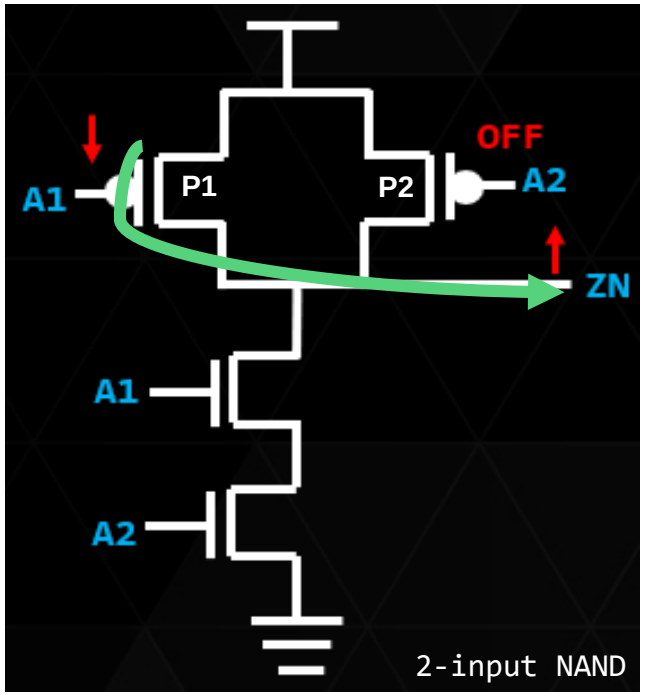
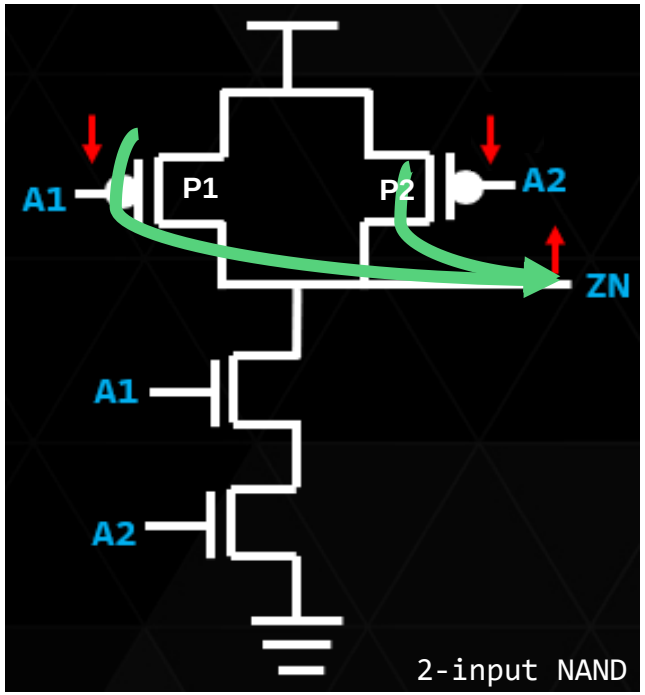
Tezaswi Raja, Reecha Jajodia, Jaison Kurien, Sarvesh Sharma

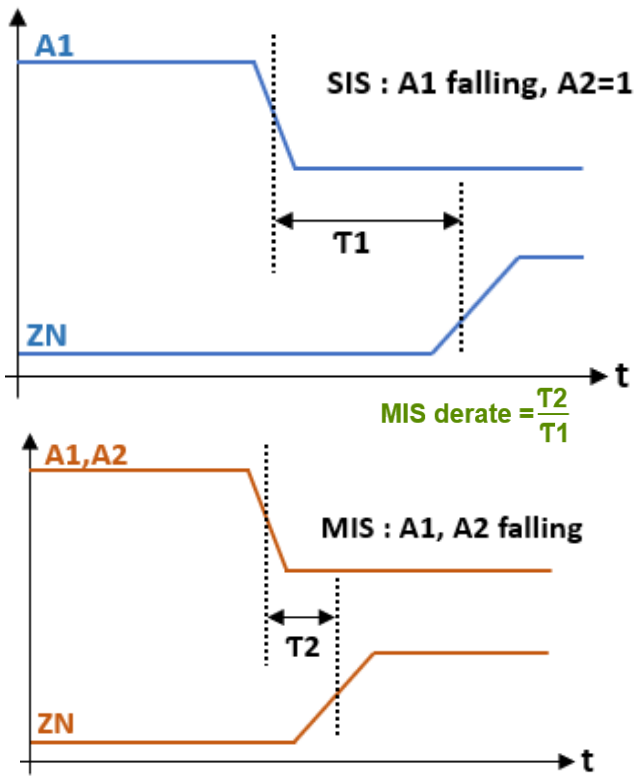
What is Multi Input Switching (MIS)?

Single Input Switching (SIS)



Multiple Input Switching (MIS)



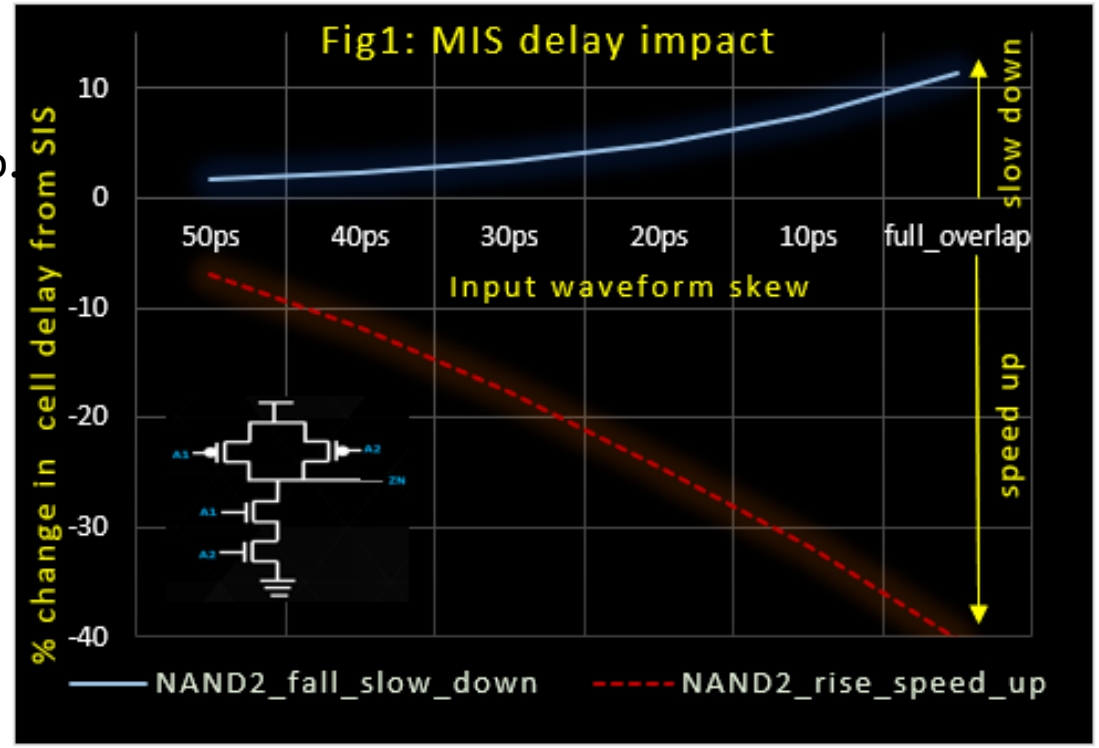


- Standard cell library timing models are SIS based.
- Does it cover real time operations?

- MIS : More than one input switching simultaneously.
- Parallel path → faster ; Series path → slower

Complexity of MIS aware timing.

- Depends on alignment of input signals, IN slew, OUT cap.
- Inaccurate assumption of arrival causes huge pessimism
- Lot of patterns to be simulated per lib-cell. High CPU cost. Huge derate DB.

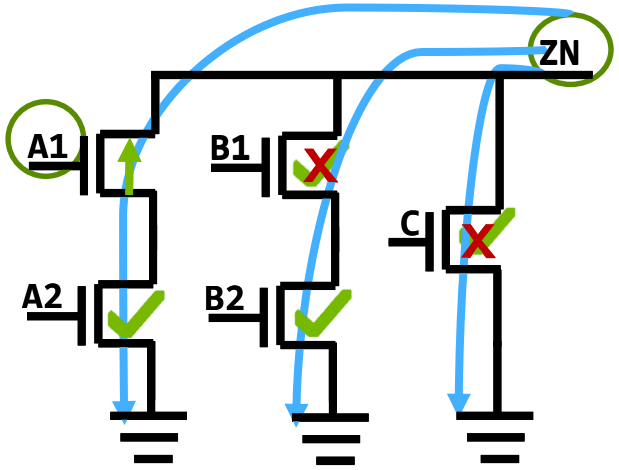


Objective of present work

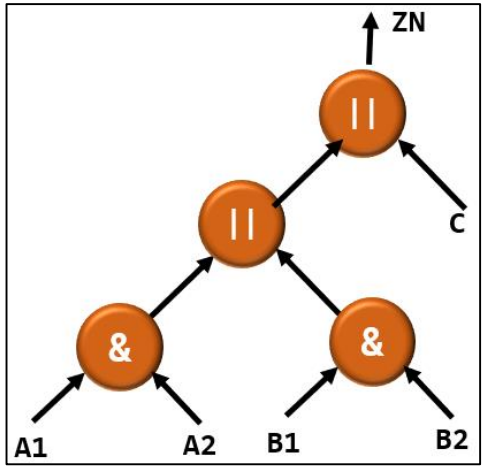
- A derate based MIS model in Static Timing Analysis.
  - ➢ Should be light weight (reduced complexity).
  - ➢ Optimal pessimism.

The Proposed Algorithm

- Input Pattern Generation : Reduced pattern
  - ➢ Find SIS patterns → Derive MIS patterns
  - ➢ Represent logic as directed cyclic graph (DAG)

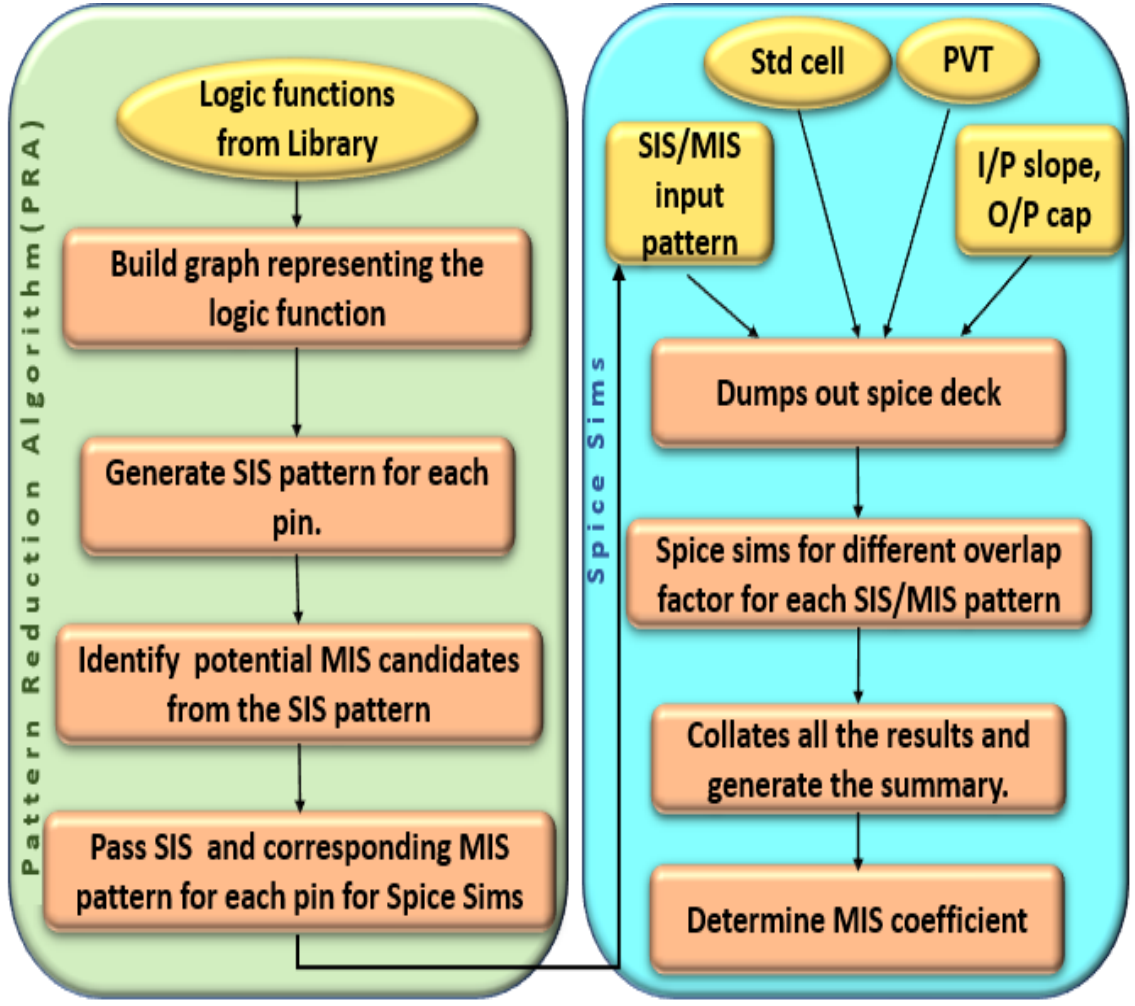


MIS pattern for A1 → ZN delay



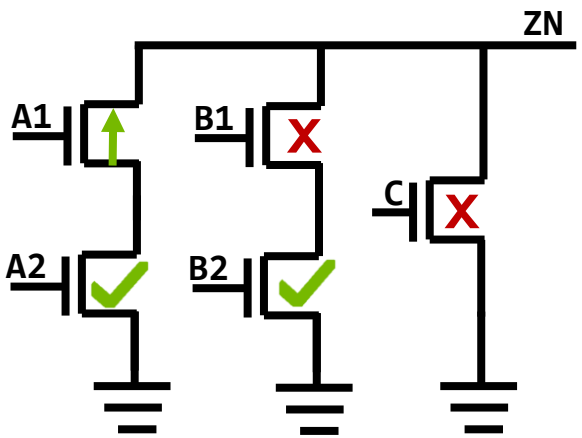
Standard cell logic DAG

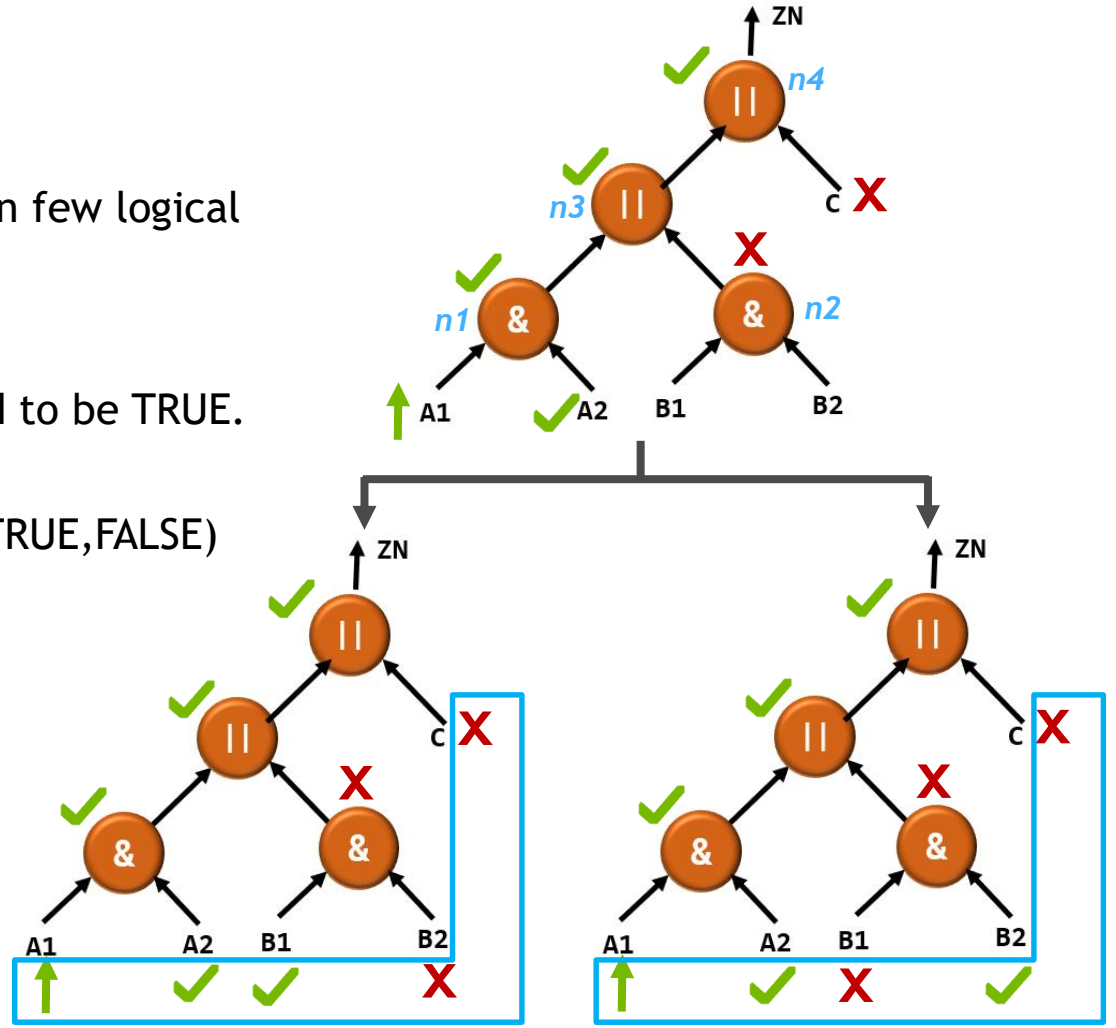
AOI221 : ((A1 & A2) || (B1 & B2)) & C



… The Proposed Algorithm

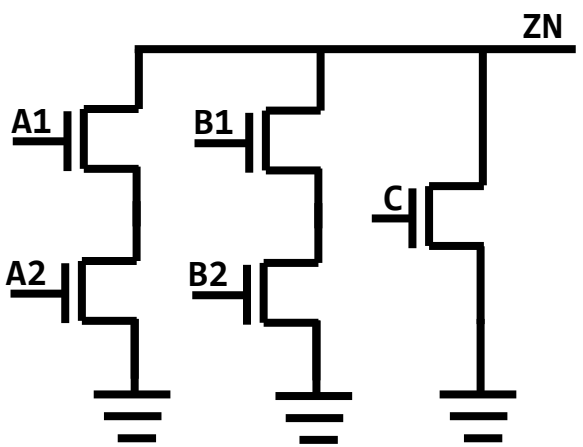
- Parse the DAG to determine SIS patterns.
- Each node is given a value TRUE or FALSE based on few logical rules . Eg:
  - For an AND to be TRUE, both the inputs need to be TRUE.
  - For an AND to be FALSE, Inputs need to be (TRUE,FALSE) or (FALSE,TRUE).





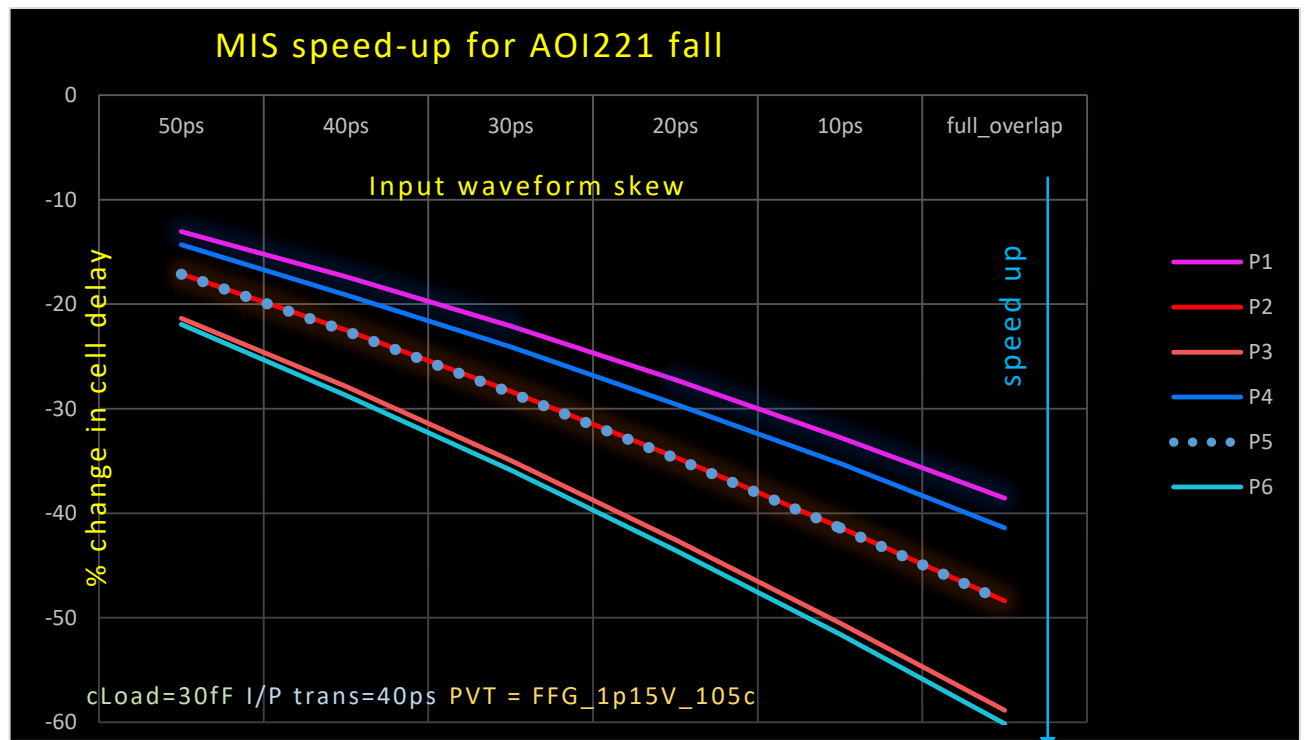
Results

- 6 reduced patterns for AOI221 for A1→ZN
- Spiced for different input waveform skew
- High MIS impact when all || paths activated : P3 and P6



AOI221 : ((A1 & A2) || (B1 & B2)) & C

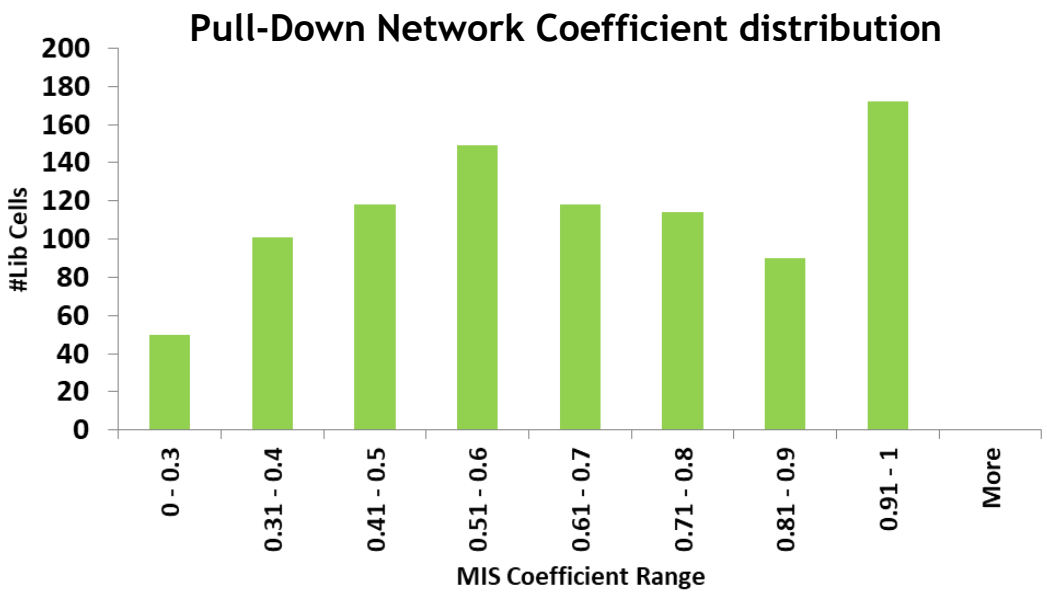
Pattern	Related Pin	MIS Impacting Pin	A1	A2	B1	B2	C1
P1	A1	B1	↑	1	↑	1	0
P2		C			0	1	↑
P3		B1 & C			↑	1	↑
P4		B2			1	↑	0
P5		C			1	0	↑
P6		B2 & C			1	↑	↑

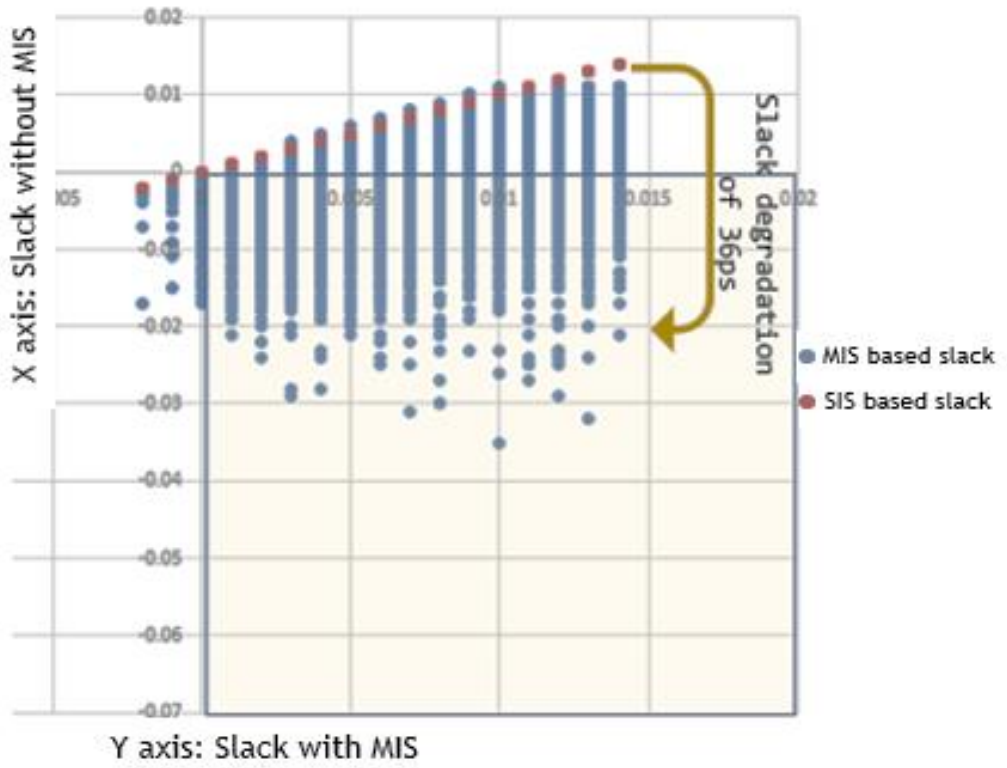


Results

MIS Coefficients(Derates) – **MIS spice delay / SIS spice delay** @ 7nm/FFG_0c_1p16V

- 4th Quadrant shows paths with negative slack with MIS.
- 0.5% paths in the design need to be reviewed and fixed.



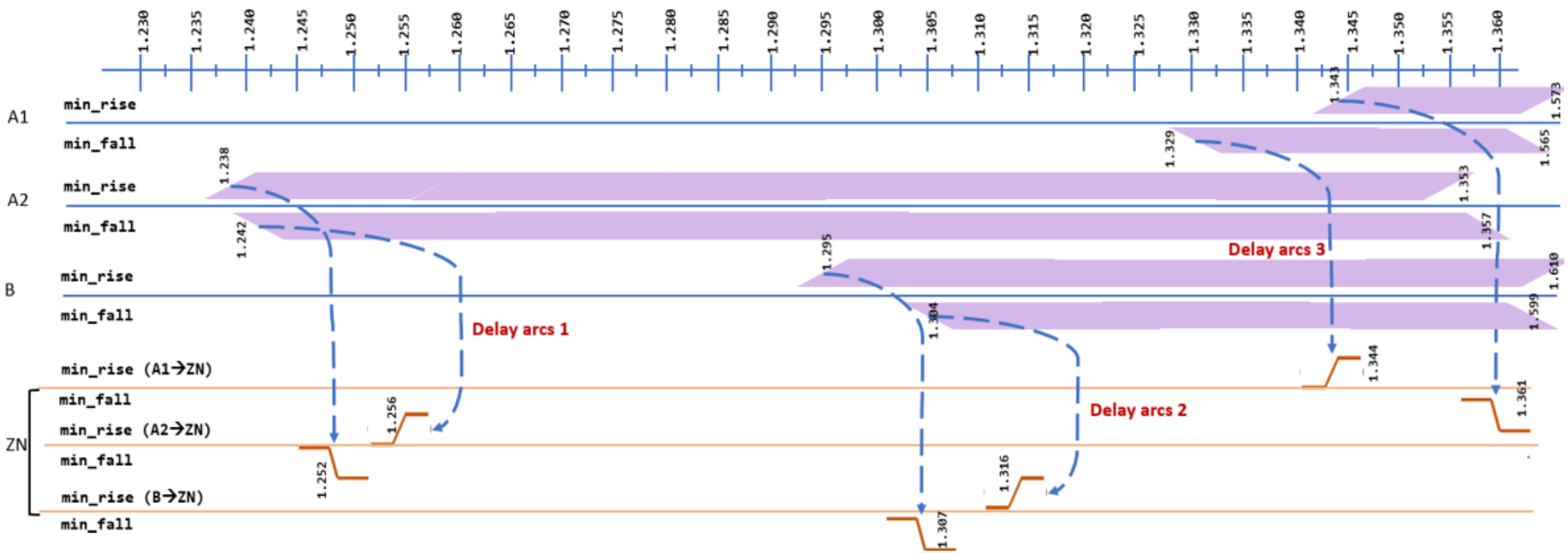


MIS impact on STA (Hold) of taped-out nVIDIA based design

Pessimism Reduction

- A lot of these paths can be pruned, deep datapath. Minimal likelihood of aligned input waveforms on all cells.

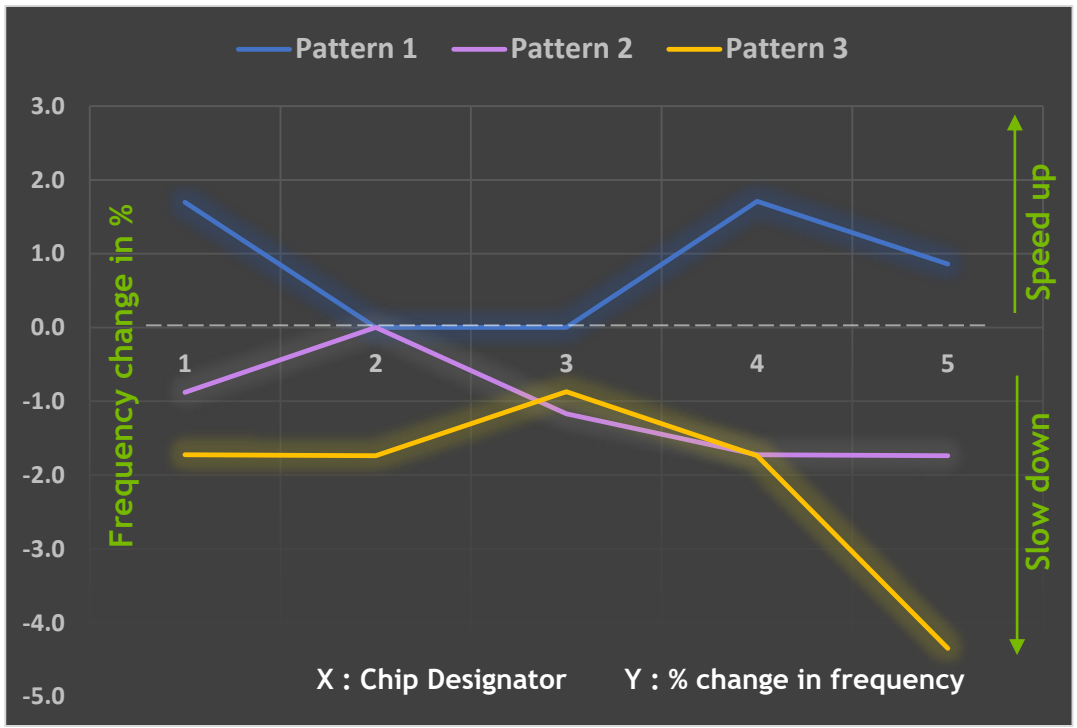
- Partial overlapping windows. For A2→ZN transition, the input waveforms at pin A1 and B are not transitioning

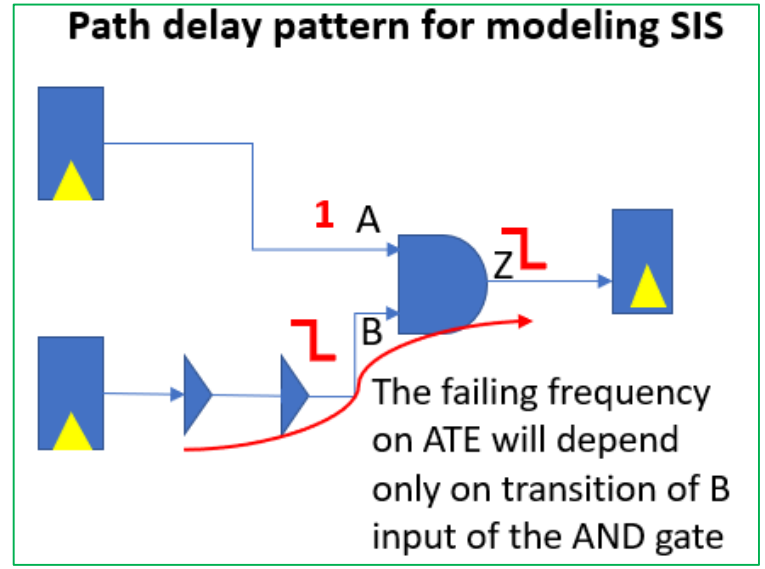


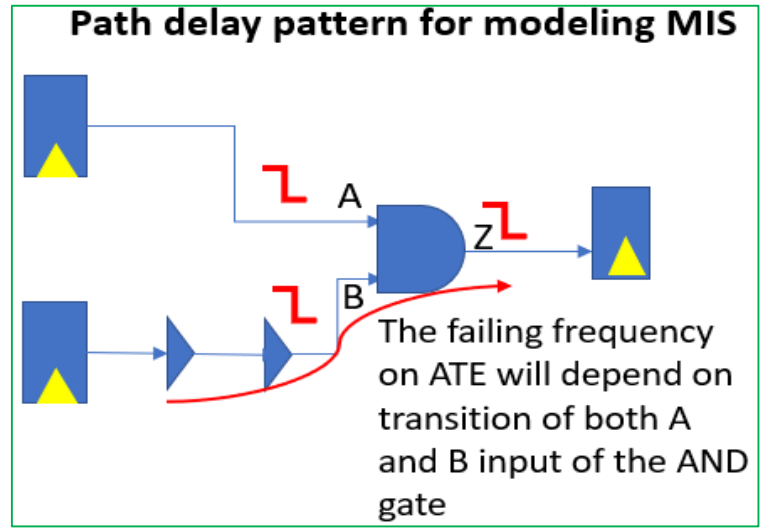
Input pins window alignment for cell AOI21

Silicon Path Frequency Correlation

- Identify MIS susceptible paths from MIS PT sessions
- Generate Pdelay patterns from TETRAMAX for SIS and MIS and generate ATE data. The silicon path delay is obtained from failing frequency for SIS and MIS







Relevance and Summary

- MIS is computationally expensive. Presented method reduces computation & memory foot print
- The algorithm supports both speed-up and slow-down.
- Arc based MIS in STA tools only cater to basic gates (30%).
- Methods presented here increases the scope to standard cells with all possible logics.

#Inputs	Logic function	#Input patterns without PRA	#Input patterns with PRA	% Reduction in #patterns
3-input NAND	!((A1&A2)&A3)	64	11	82.8
3-input AOI-21	!((A1&A2)|B)	64	10	84.4
4-input AOI-31	!(((A1&A2)&A3)|B)	256	23	91.0
4-input OAI-211	!(((A1|A2)&B)&C)	256	24	90.6
5-input AOI-221	!(((A1&A2)|(B1&B2))|C)	1024	29	97.2
5-input AOI-32	!(((A1&A2)&A3)|(B1&B2))	1024	39	96.2
6-input AOI-33	!(((A1&A2)&A3)|((B1&B2)&B3))	4096	47	98.9

Thank You !!